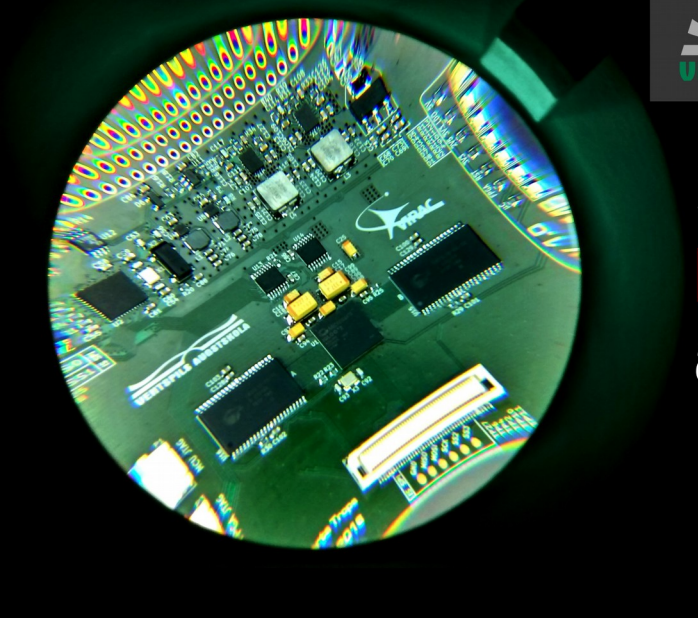

VENTSPILS AUGSTSKOLA VIRAC esa

Summer school FPGAs for SPACE applications

August 24-27, 2017
Ventspils

Invitation to Summer School "FPGAs for SPACE applications"

We cordially invite you to participate in **The Summer School "FPGAs for SPACE applications"** - a 4 day training course**.** The summer school will be held at the Ventspils University College (VUC), Latvia. The courses will comprise of both lectures and hands-on practical sessions. The Summer School will start on Thursday **August 24th** and end on Sunday **August 27th** of 2017. We hope that this event will facilitate the understanding of benefits and limitations of FPGA technology and enable workshop participants to use this knowledge to develop new high-performance satellite systems.

COURSE AIM

The purpose of this Summer School is to educate European satellite developer teams about FPGA technology and its potential in satellite applications by providing programming experience using different programming platforms.

COURSE DETAILS

Entry level: no previous knowledge on FPGA programming is required.

Background: Participants of practical sessions should preferably have engineering, computer science or any general space technology related background.

Target groups: bachelor's and master's students, graduates, lecturers and researchers form EE or IT, nanosatellite team engineers, representatives of universities and anyone interested in satellite system design.

Course organization: The course consists of 4 days of active teaching, practices and field experiences. Maximum number of participants in practical classes is 16 while in presentations and lectures there are no limitations. The working language is English.

Materials: All educational material and software (Libero SoC, LabVIEW) will be provided for free.

Other: This activity is part of ESA PECS project "Ventspils University College satellite technology education program" (Nr.4000114048/15/NL/Nde).

IMPORTANT DATES

Registration is open till **August 20th.**

FEE, ACCOMMODATION

The participation in Summer School is **FREE**, coffee and lunch will be provided by the organizers, but participants will have to cover their own travel expenses, including necessary subsistence and accommodation. Participants must book a hotel for themselves, we recommend to make all reservations well in advance, since August is tourism season in Ventspils. We recommend booking Ventspils University Colleges Hotel or somewhere near the VUC.

HOW TO APPLY

To apply for The Summer School, send us an e-mail in free form, stating:
1. Name and surname, academic degree, which institution/organization you represent.
2. Are you planning to attend only lectures, or do you want to participate in workshop?
3. When do you plan to arrive, where do you stay and how many days you plan to stay?
4. Do you have any food preferences (vegetarian, food allergies, etc) or health conditions we should know about?

E-mail to **summer_school@venta.lv**
Please specify "FPGA" in the message subject.
For any questions, please e-mail endija.briede@venta.lv

ACCOMMODATION AND TRANSPORTATION

You can find the corresponding information about accommodation at Ventspils web site: http://www.visitventspils.com/en/start/

Riga International Airport is located 13 km from the city centre which can be reached by taxi or bus. Cost per trip by taxi is approximately 15 EUR,. If you choose to take a taxi we recommend to take the green BalticTAXI. There are also regular bus connections (bus No 22) from the airport to the city centre. Regular one-way ticket in a ticket vending machine at the bus stop will cost only 1.15 EUR (http://www.riga-airport.com/en/main/passengers/useful-information/getting-to-the-airport/public-transport). More information how to get from and to Riga International Airport can be found here: http://www.riga-airport.com/en.

Ventspils (http://www.ventspils.lv/eng/) is located 190 km from Riga. The most convenient way to get to Ventspils is by bus from Riga Bus Station. Please see the bus schedule on http://www.1188.lv/transport and allow approximately 3 hours for the trip. There is also a direct Ventspils – Nynäshamn Stena Line ferry link.

Participants are responsible for their own transportation to and from Ventspils, Latvia, as well as for hotel arrangement and costs.

THE SUMMER SCHOOL SCHEDULE

Small changes to the schedule can be appended.

Day 1, Aug 24, Thu	
Registration	8:30-9:00
Summer school opening	9:00-9:15
Presentation- guest lecturer TBA	9:15-10:45
Coffee break	10:45-11:15
Presentation- FPGA space applications (lecturer J.Šate)	11:15-12:30
Lunch	12:30-13:30
Presentation- FPGA mother board design for a CubeSat (lecturer R.Trops)	13:30-14:00
Lecture- Introduction to FPGA programming in VHDL I (lecturer J.Šate)	14:00-15:00
Trip to Irbene Radiotelescopes	15:00-17:30

Day 2, Aug 25, Fri	
Presentation- guest lecturer TBA	9:00-10:00
Coffee break	10:00-10:30
Lecture- Introduction to FPGA programming in VHDL II (lecturer J.Šate)	10:30-11:30
Workshop- FPGA programming in VHDL using Libero SoC I (lecturer J.Šate)	11:30-12:30
Lunch	12:30-13:30
Workshop- FPGA programming in VHDL using Libero SoC II (lecturer J.Šate)	13:30-15:00
Coffee break	15:00-15:30
Workshop- FPGA programming in VHDL using Libero SoC III(lecturer J.Šate)	15:30-17:00

Day 3, Aug 26, Sat	
Presentation- guest lecturer TBA	9:00-10:00
Coffee break	10:00-10:30
Lecture- Digital system design with FPGA I (lecturer J.Šate)	10:30-11:30
Workshop- Digital system design with FPGA II(lecturer J.Šate)	11:30-12:30
Lunch	12:30-13:30
WorkshopParallel computing with FPGA I (lecturer J.Šate)	13:30-15:00
Coffee break	15:00-15:30
Parallel computing with FPGA II (lecturer J.Šate)	15:30-17:00

Day 4, Aug 27, Sun	
Lecture- Introduction to LabVIEW programming I (lecturer M.Donerblics)	9:00-10:00
Coffee break	10:00-10:30
Lecture- Introduction to LabVIEW programming II (lecturer M.Donerblics)	10:30-11:30
Workshop- LabVIEW FPGA programming I (lecturer M.Donerblics)	11:30-12:30
Lunch	12:30-13:30
Workshop- LabVIEW FPGA programming II(lecturer M.Donerblics)	13:30-14:30
Summer school closing remarks	14:30-15:00

LECTURER BACKGROUND

The lecturers list will be updated.

J.Šate – Lecturer and acting researcher at Ventspils University College, PhD student at University of Latvia. Expertise in FPGA based digital system design, particulary in systolic computation and digital baseband processing systems. He has been part of the team developing and testing ADCS system for ESTCube-, currently is a part of VIRAC satellite technology department.

R.Trops - Electronics engineer and acting researcher in VIRAC satellite technology department. Hardware architecture and schematic designer for High Speed Communication Subsystem (HSCOM) of ESTcube-2. Fields of expertise also include satellite radio communication channel simulations, software defined radios (SDRs) and embedded software development.

M.Donerblics – Electronics Engineer at VIRAC. Lecturer at VUC (LabVIEW programming; CAD PCB design). Developed experimental setup control and dataloging solutions for research at Paul Scherrer Institute (Switzerland) Has experiance in development of electronic systems for satellites (including communications) gained both trough Bachelors and Masters thesis as well as by participating in several projects.

LOCAL ORGANIZING COMMITTEE:

Dr. phys. Māris Ēlerts (maris.elerts@venta.lv)

Mg.sc.ing. Endija Briede (endija.briede@venta.lv)

Mg.sc.comp. Dace Briede (dace.briede@venta.lv)